



Why KIOXIA's TLC 3D BiCS FLASH™ outperforms 2D MLC flash technology

One of the most critical elements of any embedded application is its memory. After all, it's where the program and the stored data all go. No wonder that engineers spend so much time during product development in the selection of this core component.

In order to pack more data into each device, flash memory manufacturers have turned to storing more than one bit of data in each cell of memory. In 2D planar memory designs this provided the industry with a way of expanding memory capacity without increasing the die size. It was, however, not without some incurred cost.

As design engineers are well-aware, flash memory wears out as its cells are erased and written. This means that the lifetime of flash memory is limited. Storing several bits of data per cell, using Multi-Level Cell (MLC) techniques, causes the memory cell to wear out faster than when using a Single-Level Cell (SLC) technique that stores one bit per cell.

As a result, application areas with lifetime expectations of more than a decade, and those in the areas of high reliability and robustness, became reluctant to use anything other than SLC flash technology.

KIOXIA e-MMC Storage for Data-Intensive Driving

To overcome the need to simply make larger die using 2D planar approaches, [KIOXIA](#), the inventor of flash memory, launched 3D flash technology. Instead of relying on ever finer fabrication processes to deliver more memory cells per die, this new technique went into the third dimension. Starting with a 48-layer demonstration device, it became clear that this was a significant step in improving capacity limitations.

In addition, these first devices also stored several bits per cell using a Triple-Level Cell (TLC) approach. This was made possible in part thanks to another change in flash cell design that occurred at the same time, as explained in our most recent white paper.

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Traditionally, 2D planar flash uses a polycrystalline floating gate with an isolating oxide to the conductive channel that is quite thick by today's standards. 3D BiCS FLASH™ uses a silicon-nitride isolator (charge trap) technology that is thinner and less sensitive to degradation effects. Thanks to the reduced two-dimensional pressure of the designs, the memory cells can also be larger as the capacity benefits are realized in the vertical dimension.

Reliable TLC KIOXIA is committed to

As a result, 3D BiCS FLASH™ using TLC provides a comparable lifetime to 2D MLC alternatives. Thus, design engineers can specify it with confidence in their designs. For applications where the highest levels of reliability are required, some memory solutions still offer partitions using SLC, providing assurance when storing critical code sections, such as bootloaders.

It is clear that the multi-bit approach to storing data in flash memory is a long-term trend, even with 3D flash memory structures, and not a short-term fad. KIOXIA has recently started with the construction of the new [Fab7 facility at the Yokkaichi Plant](#) in the Mie Prefecture, Japan. This will expand production on a site that is already

recognized as offering the world's largest flash memory production capacity.

The use of techniques that store multiple bits per cell, such as TLC, to provide design engineers and consumers with the enormous memory capacities they are demanding will continue. Thanks to all the advancements in flash memory technology that KIOXIA is developing, you can be sure that your application's memory will stand the test of time.

Find out more about KIOXIA's BiCS FLASH™ 3D flash memory technology [here](#)

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