



## Why Replace Embedded NOR Flash Memory with Serial NAND?

More Intelligent Application Software, Advanced IoT-IIoT Devices and Faster Communication Protocols are Driving the Need for Cost-Effective, Larger Density Code Storage

Design engineers who develop innovative devices for our personal use (e.g., smart TVs, digital cameras, portable games and wearables), for the industrial and communication sectors (e.g., POS systems, robots, GPON modules and smart meters), and for next-generation applications (e.g., autonomous vehicles, video surveillance and medical imaging), need more storage for code execution.

This requirement is being driven by more compute-intensive applications including artificial intelligence, machine learning and analytical algorithms. It is also being driven by significant advancements in IoT and IIoT technologies, particularly relating to edge computing, machine to machine communications, and devices that perform continuous, real-time video/audio capture. Faster communication protocols are also driving this trend and feature more robust interfaces (such as 5G, WiFi and GPON). When all of these factors are combined with larger firmware sizes, syslog data and boot codes, the need for larger device storage densities for code execution is obvious.

At present, embedded device memory for code storage has been relegated to NOR flash memory (NOR) or NAND flash memory (NAND). NOR flash memory is a circuit architecture where the memory cells are connected in parallel between the internal bit line and ground. There is a single transistor between the internal bit line and ground to enable a low on-state resistance. As a result, NOR flash memory can perform very fast read operations making it well-suited for executing low-level code and for small applications using a command line driven interface. In addition to initializing operating systems and applications, boot-ups also include initializing diagnostics, peripherals, communications channels, DRAM channels and a variety of other processor settings.

NAND flash memory is also a memory circuit architecture, but one which delivers much larger embedded storage densities at significant bit cost savings. The memory cells are serially connected between the bit lines and ground, and anywhere from 16 to 64 transistors in series enables the elimination of the ground connection for each transistor, reducing the size of the memory array. Utilizing identical lithography, a NOR flash memory array is about 2.5x larger than the NAND flash memory array. These factors make NAND flash memory much cheaper to produce than NOR, with cost savings reflected in its pricing and in bit costs. With its primary benefit of higher density scaling than NOR flash memory, NAND also erases and writes new data faster than NOR<sup>1</sup> and delivers cost benefits<sup>2</sup> that procurement professionals strive for, helping to validate a NOR replacement strategy.

In compute-based systems, fast OS code execution and boot-ups are important, but for mobile apps where the visual interface takes time to initialize – boot-ups are not as critical. With the trend toward larger operating systems and code storage, device designers are moving away from embedded NOR flash memory as storage densities are limited and bit costs are much higher when compared to NAND.

### Delivering Larger Storage Densities

Historically, NOR flash memory and EEPROMs (electrically erasable programmable read-only memory) have provided basic, low-level application code storage for initialization and boot-ups. Depending on the size of the application, OS and other initialization data, NOR flash memory accommodated code storage with 64 megabit<sup>3</sup> (Mb), 128Mb, 256Mb and 512Mb capacities. Given today's use cases, the requirements for application code storage have reached one gigabit<sup>3</sup> (Gb) or greater in capacity. *This is a primary reason why device designers are moving away from embedded NOR, as single-level cell (SLC) NAND is the only flash memory available that cost-effectively supports 1Gb+ capacities and the code storage needs of many target applications.* As applications, operating systems and initialization data grow in size, today's cost-effective code storage capacities for target applications using serial NAND flash memory typically range from 1Gb to 4Gb, with some applications requiring 8Gb capacities (Figure 1).

## SLC NAND Target Applications

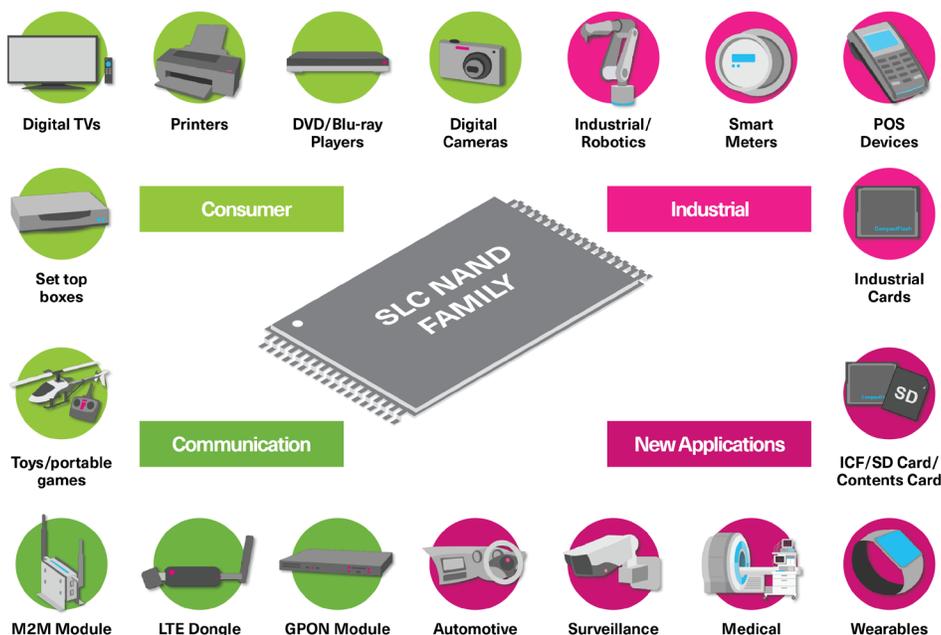


Figure 1: applications and devices targeted for SLC NAND

## Reducing Device and Bit Costs

Parallel interfaces use multiple wires that run in parallel to each other to transmit data simultaneously, where serial interfaces use a single wire to transmit data one bit at a time. As microprocessors get smaller in size, and more embedded functionality is being designed into smaller devices, the size of the storage media can be a differentiating factor as it relates to manufacturing costs. The microcontroller die must be larger to support the high pin count parallel interfaces which are driving device designers to replace them with serial interfaces. One of the most common is the Serial Peripheral Interface (SPI)<sup>4</sup>.

SPI is a synchronous serial interface specification used in embedded systems for short-distance communications that has become a de facto standard since its introduction in the mid-1980s. The interface is included with most general host processors and sends data between microcontrollers and embedded flash memory via an SPI controller. Embedded flash media based on SPI, NOR or NAND requires only eight traces to the processor where the equivalent parallel solution could require as many as 23, and more real estate on the PCB. Traces in SPI can also be considerably larger than NOR, providing more design and reliability options for circuit designers.

<b>SPI NOR flash memory capacities</b>	64Mb, 128Mb, 256Mb, 512Mb, 1Gb, 2Gb
<b>SPI NAND flash memory capacities</b>	1Gb, 2Gb, 4Gb, 8Gb

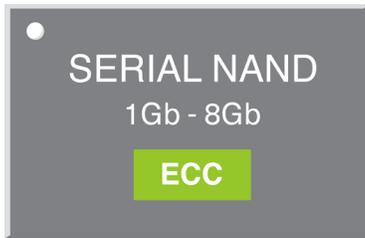
Embedded SPI NAND flash memory provides benefits such as low pin count and smaller package dimensions when compared to parallel NOR and NAND flash memory, with obvious device design and PCB cost savings. As an example of the cost benefit<sup>2</sup>, 256Mb NOR flash memory sells for roughly \$4.00<sup>2</sup> versus 1Gb NAND flash memory which sells for \$1.00<sup>2</sup>. At the device level, there is a 4x cost savings and ~4x larger capacities when NAND flash memory is used.

From a cost per bit perspective, 256Mb NOR at \$4 each equates to \$0.0156 per Mb (\$4 / 256Mb). Serial NAND with 1Gb<sup>5</sup> capacity at \$1 each equates to \$0.001, providing a cost per bit advantage over 15.5x.

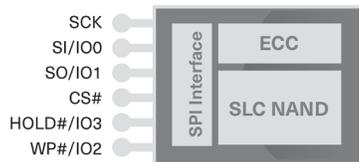
## Summary

Today's serial NAND market is primarily driven by the growing demands of many industrial and consumer applications requiring more code and data storage. As device developers seek high-density embedded memory solutions that can provide storage at the lowest available cost per gigabit, demand for embedded serial NAND flash memory is increasing. It provides the best of both worlds when compared to NOR – higher code storage densities and lower bill of materials costs.

KIOXIA Corporation (formerly Toshiba Memory Corporation) is the original developer of NAND flash memory and provides embedded SLC NAND flash memory solutions:



\* The ECC logic in Serial Interface NAND can be enabled and disabled by the customers.



## KIOXIA Serial NAND Flash Memory Key Features and Benefits

- KIOXIA's cost effective 24nm process technology
- Embedded ECC engine that customers can enable and/or disable - includes ECC Bit Flip Report
- Capacities: 1Gb, 2Gb, 4Gb, and **new** 8Gb
- Max Clock Frequency: 133MHz
- Program Mode: x1 and x4 modes
- Package Size: 6 x 8mm WSON8
- Operation Temperature: - 40°C to 85°C
- Voltages: 1.8V and 3.3V options available
- Design Registerable

For more information on KIOXIA SLC NAND flash memory, visit <https://business.kioxia.com/en-us/memory.html>.

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In every mention of a KIOXIA product: Product density is identified based on the density of memory chip(s) within the Product, not the amount of memory capacity available for data storage by the end user. Consumer-usable capacity will be less due to overhead data areas, formatting, bad blocks, and other constraints, and may also vary based on the host device and application. For details, please refer to applicable product specifications. The definition of 1KB = 2<sup>10</sup> bytes = 1,024 bytes. The definition of 1Gb = 2<sup>30</sup> bits = 1,073,741,824 bits. The definition of 1GB = 2<sup>30</sup> bytes = 1,073,741,824 bytes. 1Tb = 2<sup>40</sup> bits = 1,099,511,627,776 bits.

All other company names, product names and service names may be trademarks or registered trademarks of their respective companies.

### NOTES:

<sup>1</sup> Source: TechTarget - <https://searchstorage.techtarget.com/definition/NOR-flash-memory#:~:text=NOR%20flash%20is%20faster%20to,control%2C%20address%20and%20data%20information.>

<sup>2</sup> Based on internet pricing from leading embedded flash memory distributors as of this publication date.

<sup>3</sup> Definition of capacity - KIOXIA Corporation defines a megabyte (MB) as 1,000,000 bytes, a gigabyte (GB) as 1,000,000,000 bytes and a terabyte (TB) as 1,000,000,000,000 bytes. A computer operating system, however, reports storage capacity using powers of 2 for the definition of 1Gbit = 2<sup>30</sup> bits = 1,073,741,824 bits, 1GB = 2<sup>30</sup> bytes = 1,073,741,824 bytes and 1TB = 2<sup>40</sup> bytes = 1,099,511,627,776 bytes and therefore shows less storage capacity. Available storage capacity (including examples of various media files) will vary based on file size, formatting, settings, software and operating system, and/or pre-installed software applications, or media content. Actual formatted capacity may vary.

<sup>4</sup> The Serial Peripheral Interface (SPI) was developed by Motorola, Inc. in the mid-1980s.

<sup>5</sup> 1Gb = 1,024<sup>3</sup> bits = 1,024Mb (1,024 \* 1,024<sup>2</sup> bits).