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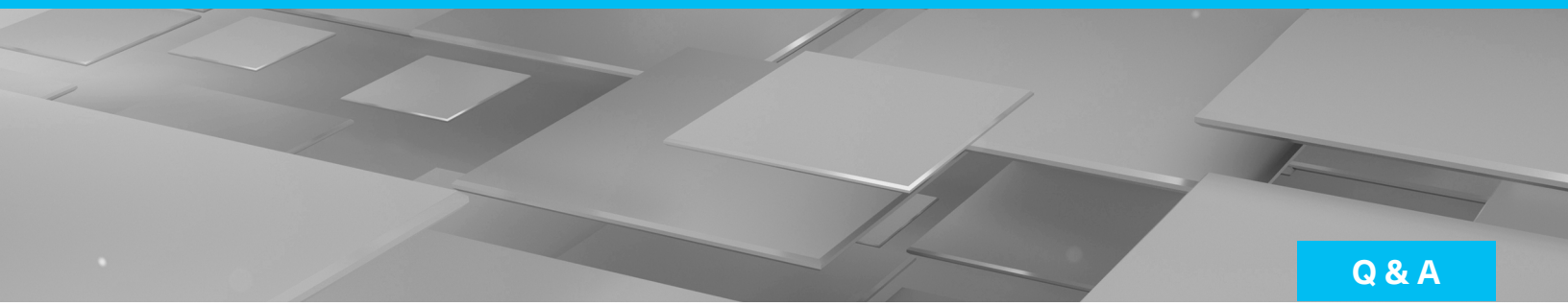

Q & A

The Layers Race: Who Really Wins?

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When it comes to technology leadership in the 3D flash memory era, what sets one supplier apart from another? If your answer has to do with number of layers, you're wrong – or at the very least shortsighted. In recent months I've had several conversations with customers and enablers about how to accurately assess performance requirements for end applications. Is it based on number of layers - or some other measurement? The answer is that a number of factors determine the NAND offering that is best suited to each application. And I'll let you in on a secret: when comparing industry 3D generation offerings, bigger, or taller, isn't always better.

Here's a recap of a recent conversation I had with an industry analyst on this topic:

Q: How does leadership in the 3D flash memory era look different than it did in the time of floating gate?

A: There are several differentiators here. First is a mindset – the industry is very accustomed to and comfortable with the predictability of 2D floating gate scaling. That is, they count on the fact that floating gate migrations/shrinks typically take 9 months to one year. For 3D flash – it is an entirely different equation. 3D migrations take from 1-1.5 years.

In floating gate, shrinking lithography also enabled a lower cost per bit – by as much as 20-25%. Contrast that to 3D, where a higher layer count and increased manufacturing complexity mean that 3D flash does not follow floating gate cost down from generation to generation.

In fact, 3D is 5-6x more CapEx intensive than floating gate, due to the new equipment it requires (including etch and deposition machines) and an increased production throughput time.

Q: Why is number of layers a non-starter when it comes to choosing a 3D flash memory supplier?

A: If reaching x amount of layers is a supplier's main goal and sole focus, it can oftentimes result in a non-competitive part. The higher number of layers and complexity inherent in a 3D solution means that managing yield becomes increasingly challenging and can come at a cost. Combine that with the aforementioned cost/performance hurdles that 3D presents, and suppliers risk losing the forest for the trees if they focus on winning the layers race.

The 3D generation to generation sweet spot for cost/performance should be evaluated per supplier – some may find that the most competitive solution can come from fewer layers.

Q: If layers aren't the key factor – what criteria should be used to define 3D flash technology leadership?

A: Simply put - meeting the performance roadmap with a competitive solution.

Let me explain. As performance increases, the manner in which each supplier delivers a part that meets specifications will be different. For example, with previous 3D generations, some suppliers were able to do so with 64 layers, and others used up to 72 layers. More recent generations are seeing from 92 to 96 layers being used.

Supporting the market's performance expectations while also optimizing CapEx investments is the key. To meet changing market performance expectations, industry suppliers consider their internal tradeoffs of squeezing a bit more from current investments vs. additional CapEx investments – a consideration which plays a part in layer count. For this reason, we see 3D generations with similar performance and different numbers of layers.

Q: What factors contribute to meeting 3D flash memory's performance roadmap?

A: The 5 keys to successfully meeting the performance roadmap are:

Interface Speed: Higher NAND interface speed will enable higher bus speed (such as PCIe 4.0).

Performance: Sequential read/write performance improvements generation over generation. Include new features to improve random read performance over traditional multi-plane read.

Reliability: Number of write/erase cycles, data retention, ECC capability requirement.

Power: Through the years, IO voltage has migrated from 3V to 1.8V – and more recently to 1.2V to help with higher interface speed and better power efficiency.

Cost: Continued innovation using different approaches to keep cost down. For example, increasing layer count, improving memory hole density, and increasing number of bits per cell, as seen in the migration from SLC technology to MLC to TLC and now to QLC.

Q: Any closing thoughts?

A: Because 3D NAND development is so different than floating gate, the industry needs to be thinking differently about 3D NAND development and the 'cost down' driven by process migration - not be defined solely by the number of layers.

When customers are evaluating who they are going to align with for their designs, they should not assume that the supplier with the highest number of layers is leading and the others are lagging behind technology-wise. Quite the opposite is more likely to be true. Getting to the most layers the fastest is far less important than producing a competitive, cost-efficient part.

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